CLAIMS

What is Claimed is:

1. A display driver comprising:

a first reference current source and a second reference current source both for supplying a reference current;

a first current-input transistor of a first conductive type including a control portion, a second impurity diffusion layer and a first impurity diffusion layer connected to the first reference current source;

a second current-input transistor of the first conductive type including a control portion, a second impurity diffusion layer and a first impurity diffusion layer connected to the second reference current source;

a plurality of mirroring devices to which currents fed to the first current-input transistor and the second current-input transistor are distributed and which are composed of transistors of the first conductive type including control portions connected to one another; and

current adding means connected to the plurality of mirroring devices for changing the output current by adding currents produced in the mirroring devices selected from among the plurality of mirroring devices in accordance with display data,

wherein the display driver is integrated on a chip.

2. The display driver of Claim 1, wherein

the plurality of mirroring devices are placed between the first current-input transistor and the second current-input transistor.

3. The display driver of Claim 2, further comprising:

a first transistor of a second conductive type which is supplied at one end with a supply voltage and connected at the other end to a resistor, thereby producing a current of a predetermined value,

wherein the first reference current source and the second reference current source are

equal in size ratio to each other and are transistors constituting a current mirror circuit in conjunction with the first transistor.

4. The display driver of Claim 3, wherein

the first reference current source and the second reference current source are placed in the vicinity of each other, and

the length and width of a wire via which the first reference current source is connected to the first current-input transistor are substantially the same as those of a wire via which the second reference current source is connected to the second current-input transistor.

5. The display driver of Claim 3, wherein

resistor elements each having an equal resistance value are further provided between the control portion of one of the plurality of mirroring devices adjacent to the first current-input transistor and the control portion of the first current-input transistor, between the control portions of each two of the plurality of mirroring devices adjacent to each other, and between the control portion of one of the plurality of mirroring devices adjacent to the second current-input transistor and the control portion of the second current-input transistor, respectively.

6. The display driver of Claim 3, further comprising:

a third reference current source that is placed between the first reference current source and the second reference current source, constitutes a current mirror circuit in conjunction with the first transistor and is composed of a transistor equal in size ratio to each of the first reference current source and the second reference current source; and

a third current-input transistor of the first conductive type that is connected to the third reference current source, is placed in the approximately central portion between the first current-input transistor and the second current-input transistor and constitutes a current mirror circuit in conjunction with the plurality of mirroring devices.

7. The display driver of Claim 3, wherein

a fourth reference current source constituting a current mirror in conjunction with the first transistor and composed of a transistor equal in size ratio to each of the first reference current source and the second reference current source, and a current-transfer terminal connected to the fourth reference current source are further provided on the same chip as the first transistor, and

a resistor connected to the first transistor is provided on the same chip as the first transistor.

8. The display driver of Claim 3, wherein

a first current-input/output terminal for transferring a reference current, a second transistor of the first conductive type including a second impurity diffusion layer, and a first impurity diffusion layer and a control portion both connected to the first current-input/output terminal, and a third transistor of the first conductive type including a second impurity diffusion layer, a control portion, and a first impurity diffusion layer connected to the first impurity diffusion layer of the first transistor and constituting a current mirror circuit in conjunction with the second transistor are further provided on the same chip as the first transistor.

9. The display driver of Claim 8, wherein

a fourth transistor of the first conductive type cascode-connected to the second impurity diffusion layer of the second transistor and a fifth transistor of the first conductive type constituting a current mirror circuit in conjunction with the fourth transistor are further provided on the same chip as the first transistor.

10. The display driver of Claim 8, wherein

a second current-input/output terminal connected to the first impurity diffusion layer of the first transistor and the first impurity diffusion layer of the third transistor, a fourth reference current source composed of a transistor that constitutes a current mirror in conjunction with the first transistor and is equal in size ratio to each of the first reference current source and the second reference current source, and a current-transfer terminal

connected to the fourth reference current source are further provided on the same chip as the first transistor.

11. The display driver of Claim 1, wherein

the first reference current source, the second reference current source, the first current-input transistor, the second current-input transistor, and the plurality of mirroring devices are MOSFETs having a first impurity diffusion layer serving as a drain, a second impurity diffusion layer serving as a source and a control portion serving as a gate electrode.